MC100LVELT23

3.3 V Dual Differential LVPECL/LVDS to LVTTL Translator

ON Semiconductor®

http://onsemi.com

Description

The MC100LVELT23 is a dual differential LVPECL/LVDS to LVTTL translator. Because LVPECL (Positive ECL) or LVDS levels are used only +3.3 V and ground are required. The small outline 8-lead package and the dual gate design of the LVELT23 makes it ideal for applications which require the translation of a clock and a data signal.

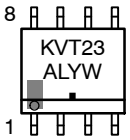
The LVELT23 is available in only the ECL 100K standard. Since there are no LVPECL outputs or an external V_{BB} reference, the LVELT23 does not require both ECL standard versions. The LVPECL inputs are differential. Therefore, the MC100LVELT23 can accept any standard differential LVPECL input referenced from a V_{CC} of +3.3 V.

Features

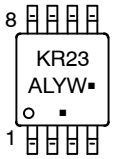
- 2.0 ns Typical Propagation Delay
- Maximum Frequency > 180 MHz
- Differential LVPECL Inputs
- PECL Mode Operating Range: V_{CC} = 3.0 V to 3.8 V with GND = 0 V
- 24 mA LVTTL Outputs
- Flow Through Pinouts
- Internal Pulldown and Pullup Resistors
- Pb−Free Packages are Available

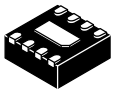
MARKING DIAGRAMS*

SOIC−8
D SUFFIX
CASE 751

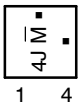


TSSOP−8
DT SUFFIX
CASE 948R





DFN8
MN SUFFIX
CASE 506AA



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
$\overline{M}$ = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

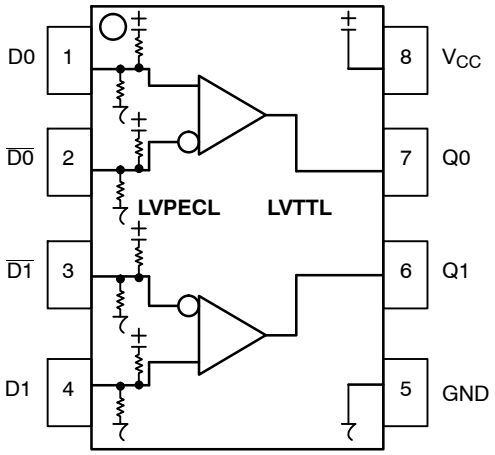


Figure 1. 8−Lead Pinout (Top View) **and Logic Diagram**

Table 1. PIN DESCRIPTION

Pin	Function
Q0, Q1	LVTTL Outputs
D0*, D1*	Differential LVPECL Inputs
$\overline{D0}$*, $\overline{D1}$*	
V_{CC}	Positive Supply
GND	Ground
EP	(DFN8 only) Thermal exposed pad must be connected to a sufficient thermal conduit. Electrically connect to the most negative supply (GND) or leave unconnected, floating open.

** Pins will default to $V_{CC}/2$ when left open.

Table 2. ATTRIBUTES

Characteristics		Value
Internal Input Pulldown Resistor		50 kΩ
Internal Input Pullup Resistor		50 kΩ
ESD Protection	Human Body Model Machine Model CDM	> 1500 V > 100 V > 2000 V
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)		Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count		91
Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. Refer to Application Note AND8003/D for additional information.

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	PECL Power Supply	GND = 0 V		3.8	V
V_I	Input Voltage	GND = 0 V, V_I not more positive than V_{CC}		3.8	V
I_{out}	Output Current	Continuous Surge		50 100	mA
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	SOIC−8 SOIC−8	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	Standard Board	SOIC−8	41 to 44 ± 5%	°C/W
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	TSSOP−8 TSSOP−8	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	Standard Board	TSSOP−8	41 to 44 ± 5%	°C/W
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	DFN8 DFN8	129 84	°C/W °C/W
T_{sol}	Wave Solder Pb Pb−Free	<2 to 3 sec @ 248°C <2 to 3 sec @ 260°C		265 265	°C
θ_{JC}	Thermal Resistance (Junction−to−Case)	(Note 2)	DFN8	35 to 40	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

2. JEDEC standard multilayer board − 2S2P (2 signal, 2 power)

Table 4. LVPECL INPUT DC CHARACTERISTICS V_{CC} = 3.3 V; GND = 0 V (Note 3)

		−40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{CCH}	Power Supply Current (Outputs set to HIGH)	10	18	25	10	18	25	10	18	25	mA
I_{CCL}	Power Supply Current (Outputs set to LOW)	15	26	36	15	26	36	15	26	36	mA
V_{IH}	Input HIGH Voltage (Note 5)	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Note 5)	1490		1825	1490		1825	1490		1825	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Notes 4 and 5)	1.2		V_{CC}	1.2		V_{CC}	1.2		V_{CC}	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current $\overline{D}$	−150			−150			−150			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

3. All values vary 1:1 with V_{CC}. V_{CC} can vary ±0.3 V.
4. V_{IHCMR} min varies 1:1 with GND, max varies 1:1 with V_{CC}.
5. LVTTL output R_L = 500 Ω to GND.

Table 5. LVTTL OUTPUT DC CHARACTERISTICS V_{CC} = 3.3 V; GND = 0V (Note 6)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage (I_{OH} = –3.0 mA) (Note 7)	2.4			2.4			2.4			V
V_{OL}	Output LOW Voltage (I_{OL} = 24 mA) (Note 7)			0.5			0.5			0.5	V
I_{OS}	Output Short Circuit Current	–180		–50	–180		–50	–180		–50	mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

6. All values vary 1:1 with V_{CC}. V_{CC} can vary ±0.3 V.
7. LVTTL output R_L = 500 Ω to GND.

Table 6. AC CHARACTERISTICS V_{CC} = 3.3 V; GND = 0 V (Notes 8, 9)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
F_{max}	Maximum Toggle Frequency (Note 10)	180			180			180			MHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential	1.0	1.5	2.5	1.0	1.7	2.5	1.0	1.7	2.5	ns
t_{SK++} t_{SK--} t_{SKPP}	Output–to–Output Skew++ Output–to–Output Skew– – Part–to–Part Skew (Note 11)		15 35 70	60 80 500		15 40 70	70 80 500		30 40 140	125 80 500	ps
t_{JITTER}	Random Clock Jitter (RMS)		4.0	10		4.0	10		4.0	10	ps
V_{PP}	Input Voltage Swing (Differential Configuration) (Note 12)	200	800	1000	200	800	1000	200	800	1000	mV
t_r t_f	Output Rise/Fall Times (0.8 V – 2.0 V) Q, $\overline{Q}$	330	600	900	330	600	900	330	650	900	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

8. All values vary 1:1 with V_{CC}. V_{CC} can vary ±0.3 V.
9. LVTTL output R_L = 500 Ω to GND and C_L = 20 pF to GND. Refer to Figure 2.
10. F_{max} guaranteed for functionality only. V_{OL} and V_{OH} levels are guaranteed at DC only.
11. Skews are measured between outputs under identical conditions.
12. 200 mV input guarantees full logic swing at the output.

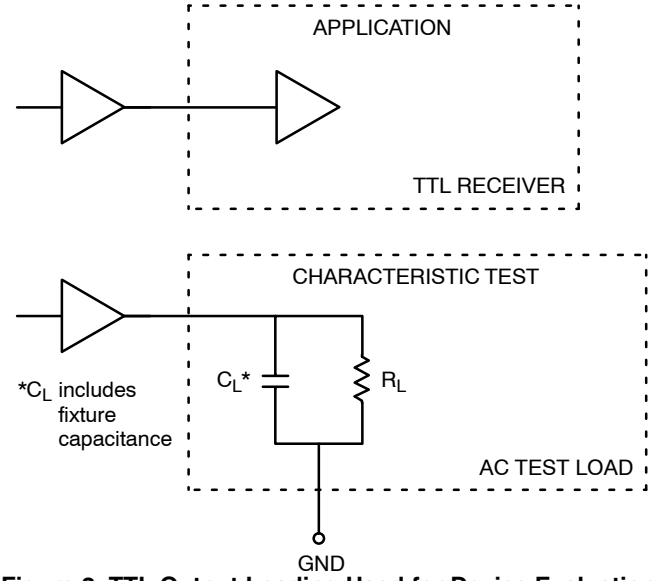


Figure 2. TTL Output Loading Used for Device Evaluation

ORDERING INFORMATION

Device	Package	Shipping†
MC100LVELT23D	SOIC−8	98 Units / Rail
MC100LVELT23DG	SOIC−8 (Pb−Free)	98 Units / Rail
MC100LVELT23DR2	SOIC−8	2500 / Tape & Reel
MC100LVELT23DR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel
MC100LVELT23DT	TSSOP−8	100 Units / Rail
MC100LVELT23DTG	TSSOP−8 (Pb−Free)	100 Units / Rail
MC100LVELT23DTR2	TSSOP−8	2500 / Tape & Reel
MC100LVELT23DTRG	TSSOP−8 (Pb−Free)	2500 / Tape & Reel
MC100LVELT23MNR4	DFN8	1000 / Tape & Reel
MC100LVELT23MNR4G	DFN8 (Pb−Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Resource Reference of Application Notes

AN1405/D – ECL Clock Distribution Techniques

AN1406/D – Designing with PECL (ECL at +5.0 V)

AN1503/D – ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D – Metastability and the ECLinPS Family

AN1568/D – Interfacing Between LVDS and ECL

AN1672/D – The ECL Translator Guide

AND8001/D – Odd Number Counters Design

AND8002/D – Marking and Date Codes

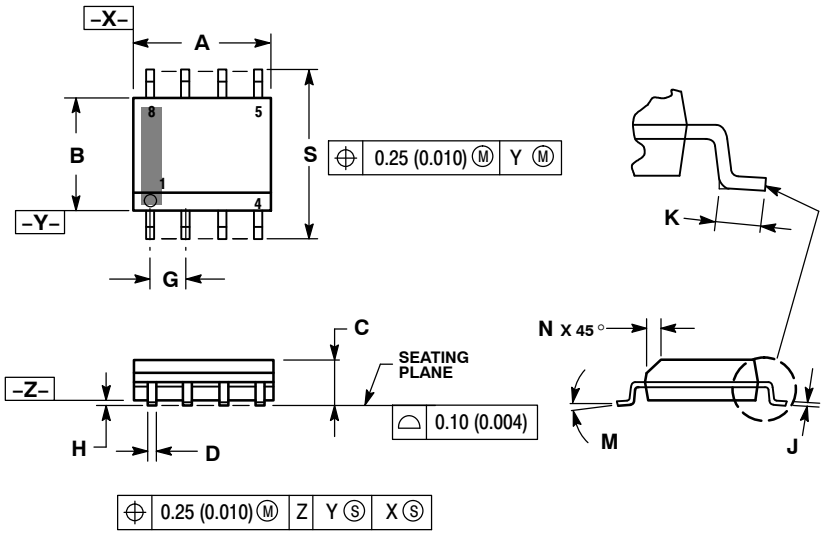
AND8020/D – Termination of ECL Logic Devices

AND8066/D – Interfacing with ECLinPS

AND8090/D – AC Characteristics of ECL Devices

PACKAGE DIMENSIONS

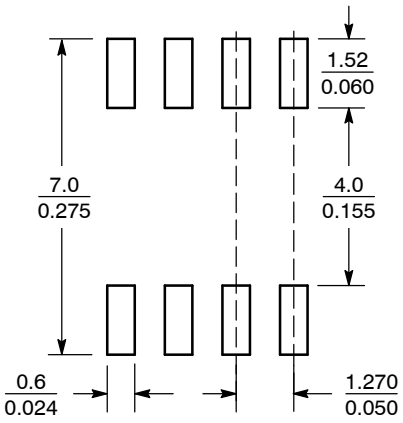
SOIC−8 NB
CASE 751−07
ISSUE AH



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*

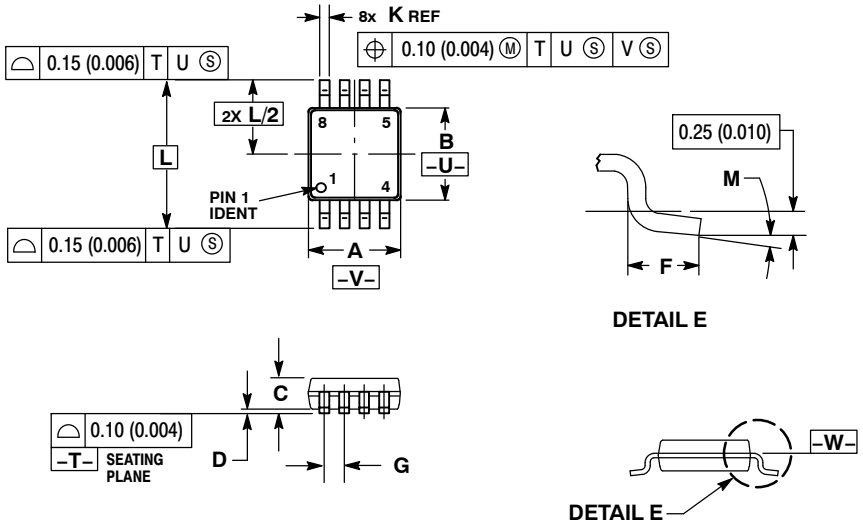


SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

TSSOP−8
DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948R−02
ISSUE A

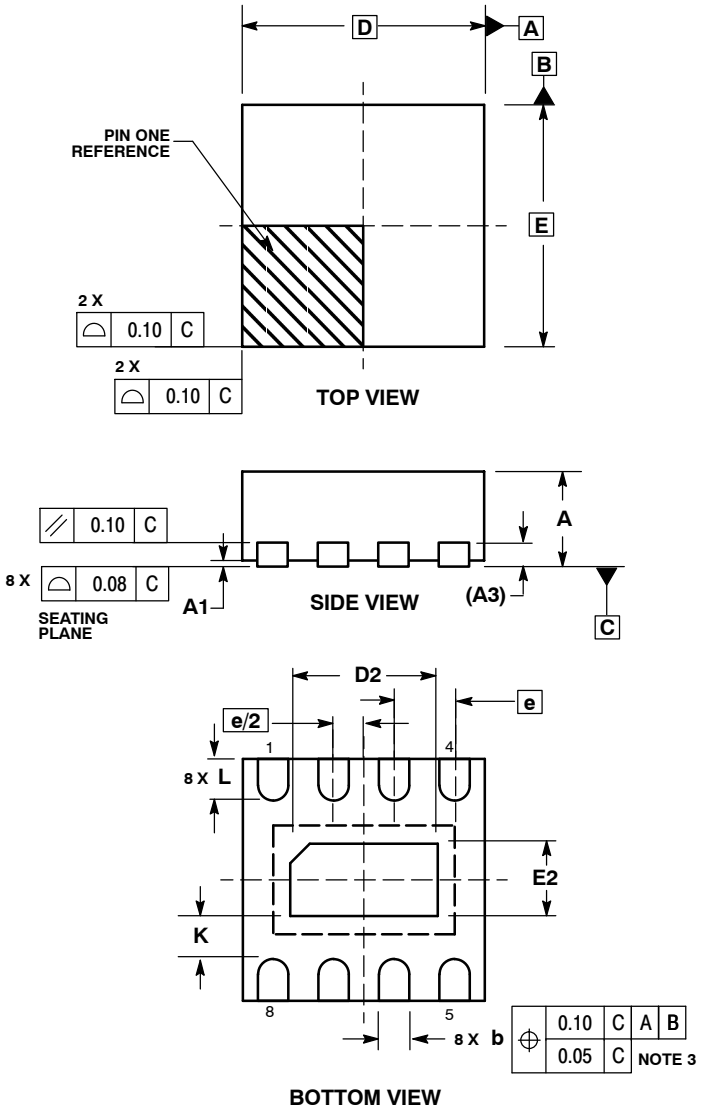


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

PACKAGE DIMENSIONS

DFN8
CASE 506AA−01
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994 .
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
D2	1.10	1.30
E	2.00 BSC	
E2	0.70	0.90
e	0.50 BSC	
K	0.20	−−−
L	0.25	0.35

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PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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